IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Michael R. Krause et al.	Examiner: George C. Neurauter
Serial No.:	09/980,920	Group Art Unit: 2143
Filed:	April 11, 2002	Docket No.: 10002166-2
Title:	MEMORY MANAGEMENT IN DISTRIBUTED COMPUTER SYSTEM	

REPLY BRIEF TO EXAMINER'S ANSWER

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Reply Brief is presented in response to the Examiner's Answer mailed August 10, 2007, and in support of the Notice of Appeal filed April 27, 2007, and the Appeal Brief filed June 27, 2007, appealing the rejection of claims 1-34 of the above-identified application as set forth in the Final Office Action mailed February 27, 2007.

At any time during the pendency of this application, please charge any fees required or credit any overpayment due to Deposit Account No. 08-2025 pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees required to Deposit Account No. 08-2025 under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Appellant respectfully requests reconsideration and reversal of the Examiner's rejection of pending claims 1-34.

ARGUMENT

The language and arguments set forth in the Grounds of Rejection section (9) of Examiner's Answer at pages 3-15 appear to be identical to the language and arguments set forth in the Final Office Action mailed February 27, 2007. Appellant has addressed these arguments in the Appeal Brief filed on June 26, 2007.

In the Response to Argument section (10) of Examiner's Answer at pages 15-18, the Examiner cites and quotes the Futral et al. patent at column 7, lines 5-17; column 5, lines 18-42; column 4, lines 31-50; and column 4, lines 51-65 to rebut Appellant's argument in the Appeal Brief that the Futral et al. patent does not teach or suggest limitations of independent claim 1 and independent claim 19 related to performing a remote direct memory access operation from a second host processor endnode with a second consumer process stored in a second memory of the second host processor endnode to access a contiguous memory address range accessible by a first consumer process stored in a first memory at a first host processor endnode, wherein the remote direct memory access operation includes sending the bound remote key and the first address from the second host processor endnode to the first host processor endnode on the communication fabric via the second NIC and the first NIC.

Appellant respectfully submits that these cited portions of the Futral et al. patent teach a method for directing transfer of input/output (I/O) of an I/O device to other processing units in a computer system including first and second processing units and an I/O unit coupled to an interconnect fabric. The second processing unit controls access to the I/O unit, which is coupled to an I/O device. **Memory fragments of the first processing unit are registered with the interconnect fabric to get memory handles for the memory fragments. A list is created having an identifier of the first processing unit, the memory handles, and virtual addresses and links of memory fragments. The list is sent from the first processing unit to the second processing unit. The list is sent from the second processing unit to the I/O unit**. The identifier of the first processing unit is examined and a communications connection from the I/O unit to the first processing unit is determined. I/O data is transferred over the communication connection between and I/O unit and memory referenced by the memory handles and virtual addresses. The method supports peer-to-peer operation where a number of different I/O units, each with its own physical memory addressing domain, require access to the same I/O device. In the embodiment specifically

described at column 5 of the Futral et al. patent referenced by the Examiner, **the combination of a platform identifier, a memory handle for registered memory, and a virtual address uniquely identifies memory located anywhere in a clustered computer system.**

Thus, the Futral et al. patent does not teach or suggest performing **a remote direct memory access operation from a second host processor endnode with a second consumer process stored in a second memory of the second host processor endnode** to access a contiguous memory address range accessible by a first consumer process stored in a first memory at a first host processor endnode, wherein the remote direct memory access operation includes sending the bound remote key and the first address from the second host processor endnode to the first host processor endnode on the communication fabric via the second NIC and the first NIC as recited in independent claims 1 and 19. By contrast, the Futral et al. patent teaches a second host system directing **an I/O device to transfer data between** a requesting application program's buffers on **a first host system and an I/O unit** coupled to the I/O device **without the need to pass through the second host system**, where the second host system retains control of the I/O request.

In the Response to Argument section (10) of Examiner's Answer at pages 19-20, the Examiner cites and quotes the Futral et al. patent at column 4, lines 31-50 and the Present Specification at page 6, lines 13-24 to rebut Appellant's argument in the Appeal Brief that a host processor endnode as recited in independent claims 1 and 19 is in no way equivalent to an I/O device or I/O unit as disclosed in the Futral et al. patent.

In the non-final Office Action mailed July 7, 2006, at page 3 in the Response to Arguments, the Examiner equates "I/O device" or "I/O unit" or "host" as interchangeable terms. As presented in the Remarks of the Amendment and Response filed December 7, 2006 in response to the July 7, 2006 non-final Office Action, these terms and their definitions in the method and computer system disclosed in the Futral et al. patent are all distinctly defined as summarized in the above remarks and in the Appeal Brief. Accordingly, a host processor endnode in independent claims 1 and 19 and as clearly defined in the Present Specification is in no way equivalent to an I/O device or I/O unit. This distinction is clear from both the Present Specification and claims and the disclosed method and computer system of the Futral et al. patent.

Now, in the Response to Argument section (10) of Examiner's Answer at page 20, the Examiner equates "unit" with "host" in the Futral et al. patent and "host processor endnode" with "endnode" in the Present Specification. In the Final Office mailed February 27, 2007, at pages 2-3 in the Response to Arguments, the Examiner disagreed with the Remarks filed by Applicant in the Amendment and Response filed December 7, 2006. The Examiner specifically refers in the Final Office Action and in the Examiner's Answer to the Futral et al. patent at column 4, lines 45-50 which states, "host systems and I/O units are generically called units. A unit may have multiple SAN NICs installed. SAN NICs attach a unit to the SAN Fabric. The SAN NIC provides connections to other units that are external to the unit." This section of the Futral et al. patent merely states there is a generic term for host systems and I/O units, but the host system is one specific type of unit and the I/O unit is another specific type of unit. **Similarly, as defined in the Present Specification, host processor endnodes (e.g., host processor endnodes 34 illustrated in Figure 1) and I/O adapter endnodes (e.g., I/O adapter endnodes 35 illustrated in Figure 1) are two specific types of endnodes as illustrated in Figure 1 and disclosed in the corresponding text of the Present Specification.** Examples in Futral et al. patent of the clear distinction between the terms host system, I/O unit, and I/O device are illustrated, for example, in Figure 1 of the Futral et al. patent where host system 10 and host system 16 are illustrated along with I/O unit 14 and I/O device 12 and also, for example, in Figure 2, where cluster host systems 20, 22, and 24 are illustrated along with I/O units 30, 32, and 34 along with corresponding I/O devices. Thus, as indicated above, host systems, I/O units, and I/O devices are separate and distinctly described and illustrated in detail in the Futral et al. patent. In addition, the Present Specification clearly defines that **host processor endnodes and I/O adapter endnodes are two specific types of endnodes.**

Accordingly, a host processor endnode as recited in independent claims 1 and 19 is in no way equivalent to an I/O device or I/O unit.

In the Response to Argument section (10) of Examiner's Answer at page 20, the Examiner states that the Futral et al. patent clearly discloses that "both the NIC and the endnode inherently contain a processor and memory to perform their respective functions." This is consistent with the Examiner's statement in the non-final Office Action mailed July 7,

2006, at page 3 in the Response to Arguments that the "SAN NIC" inherently contains a processor and memory.

Appellant, however, respectfully submits that independent claims 1 and claim 19 specifically define operations performed by a first network interface controller (NIC) in the first host processor endnode and a second NIC in the second host processor endnode. The Futral et al. patent also specifically defines functions of the SAN NICs in its described computer system. Thus, as clearly defined in independent claims 1 and 19, **the first processor and the first memory in the first host processor endnode are separate and distinct from the NIC in the first processor endnode and the second processor and the second memory in the second host processor endnode are separate and distinct from the second NIC in the second host processor endnode**.

In view of the above additional remarks responding specifically to the Examiner's Answer and the remarks in the Appeal Brief filed on June 26, 2007, the Futral et al. patent does not teach or suggest the method of independent claim 1 or the distributed computer system of independent claim 19. Therefore, the Futral et al. patent does not anticipate independent claims 1 and 19.

Furthermore, dependent claims 2-18 further define patentable distinct independent claim 1 and dependent claims 20-34 further define patentably distinct independent claim 19. Therefore, these dependent claims are also neither anticipated by the Futral et al. patent nor rendered obvious in combination with any of the cited references (see complete arguments in Appeal Brief).

Therefore, Appellant respectfully requests reversal of the rejections of claims 1-34 under 35 U.S.C. § 102 and § 103 and allowance of these claims.

CONCLUSION

For the above reasons, Appellant respectfully submits that the art of record neither anticipates nor renders obvious the claimed invention. Thus, the claimed invention does patentably distinguish over the art of record. Appellant, therefore, respectfully submits that the above rejections are not correct and should be withdrawn, and respectfully requests that the Examiner be reversed and that all pending claims be allowed.

Any inquiry regarding this Reply Brief should be directed to either Patrick G. Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005 or Kevin Hart at Telephone No. (970) 898-7057, Facsimile No. (970) 898-7247. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

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Date: October 10, 2007
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